CLAIMS:

1. A punch-through diode realized as a monolithically integrated circuit based an a silicon dice or chip, comprising an n^+-doped substrate (7) covered with an n-doped epilayer (8); a first p-well (9) and a second p-well (10) implanted into the n-doped epilayer (8) with a distance between the two wells; an n-well (11) penetrating through the n-doped epilayer (8) and into the n^+-substrate (7); a first p^+-doped well (13) which connects both the first and the second p-doped wells (9, 10); a polysilicon area (14) on the n-epilayer (8) between the first and the second n-doped wells (9, 10) overlapping the edges of an oxide layer (17); characterized in that a Schottky-metal area (16) is deposited onto at least part of the first p-doped well's (9) surface thus forming a metal (16) - semiconductor (9) -transition and that a second p^+-doped well (12) is implanted into the first p-doped well (9).

2. A punch-through diode realized as a monolithically integrated circuit based an a silicon dice or chip, comprising a p^+-doped substrate covered with a p-doped epilayer; a first n-well and a second n-well implanted into the p-doped epilayer with a distance between the two wells; a p-well penetrating through the p-doped epilayer and into the p^+-substrate; a first n^+-doped well which connects both the first and the second n-doped wells; a polysilicon area on the p-epilayer between the first and the second p-doped wells overlapping the edges of an oxide layer; characterized in that a Schottky-metal area is deposited onto at least part of the first n-doped well's surface thus forming a metal - semiconductor -transition and that a second n^+-doped well is implanted into the first n-doped well.

3. A punch-through diode according to any of the foregoing claims, characterized in that the monolithic integrated circuit is built on a wafer.

4. A punch-through diode according to any of the foregoing claims, characterized in that the Schottky-metal (16) overlaps the edges of the ambient oxide layer (17).

5. A punch-through diode as claimed in any of the foregoing claims, characterized in that the Schottky-metal area (16) is made of a material from the group comprising aluminium (Al), titanium (Ti), iron (Fe), chrome (Cr), nickel (Ni), molybdenum (Mo), palladium (Pd).

6. A punch-through diode according to any of the foregoing claims characterized in that the punch-through diode comprises a layer of aluminum on the surface of the n^+-substrate (7) or p^+-substrate to enable the contact of a first terminal point of the punch-through diode.

7. A punch-through diode according to any of the foregoing claims characterized in that the punch-through diode comprises a metallized layer above the Schottky-metal area and the polysilicon area that enables the contact to a second terminal point.

8. A punch-through diode as claimed in one of the foregoing claims characterized in that it is realized as a thick film circuit.

9. An electronic appliance, comprising a punch-through diode according to any of the former claims.

10. Use a punch-through diode according to any of the claims 1 to 8 for overvoltage protection in an integrated circuit.

11. A method of processing a punch-through diode, comprising the steps of providing an n^+-substrate (7); generating an n-epilayer (8); forming a first p-doped well (9) in the n-epilayer (8); forming a second p-doped well (10) in the n-epilayer (8);

forming an n-doped well (11) penetrating through the epilayer (8) and into the n^+-substrate (7); forming a p^+-doped well (13) in the epilayer (8) between the first and the second p-doped wells (9, 10); forming a polysilicon layer (14) between the first and the second p-doped wells (9, 10) overlapping their opposite margin edges; forming an n-doped well (15) under the surface of the epilayer (8) between the first and the second p-doped wells (9, 10); forming a Schottky-metal area (16) on the first p-doped well (9).

12. A method of processing a punch-through diode, comprising the steps of providing a p^+-substrate; generating a p-epilayer; forming a first and a second n-doped well in the p-epilayer; forming a p-doped well penetrating through the epilayer and into the p^+-substrate; forming an n^+-doped well in the epilayer between the first and the second n-doped wells; forming a polysilicon layer between the first and the second n-doped wells overlapping their opposite margin edges; forming a p-doped well under the surface of the epilayer between the first and the second n-doped wells; forming a Schottky-metal area on the first n-doped well.